Informal-Type Examiners' Amendment:
In claim 10, line 1, "5" has been changed to --6--.

CLAIMS

What is claimed is:

1. A system to calibrate an oscillator within a radio-frequency identification (RFID) circuit for use in an RFID tag, the oscillator having an oscillation frequency and the system including:

an input, associated with the RFID circuit, to receive a test signal; and

a calibration module to store a calibration value within a non-volatile memory associated with the RFID circuit,

wherein the calibration module is to recover a reference frequency from the test signal, to calculate the calibration value to correspond to a difference between the recovered reference frequency and the oscillator frequency, and to write the calibration value to the non-volatile memory.

2. The system of claim 1, wherein the input is to receive the test signal via at least one of a wired link and a radio-frequency link.

3. The system of claim 1, wherein the test signal comprises a DC power signal supplied to the RFID circuit.

4. The system of claim 1, wherein the RFID circuit operates in one of at least a programming mode and interrogation mode, and the calibration module is to store the calibration value within the non-volatile memory in the programming mode.

5. The system of claim 1, wherein the calibration module is iteratively to calculate the calibration value and to write the calibration value to the non-volatile memory.

6. A method of calibrating an oscillator within a radio-frequency identification (RFID) circuit for use in an RFID tag, the oscillator having an oscillation frequency and the method including:

storing a calibration value within a non-volatile memory associated with the RFID circuit; and

calibrating the oscillator in accordance with the calibration value,

wherein the storing of the calibration value includes recovering a reference frequency from a test signal supplied to the RFID circuit, calculating the calibration value to correspond to a difference between the recovered reference frequency and the oscillator frequency, and writing the calibration value to the non-volatile memory.

7. The method of claim 6, wherein the test signal is supplied via at least one of a wired link and a radio-frequency link to the RFID circuit.

8. The method of claim 6, wherein the test signal comprises a DC power signal supplied to the RFID circuit.

9. The method of claim 6, wherein the RFID circuit operates in one of at least a programming mode and interrogation mode, and the storing of the calibration value within the non-volatile memory is performed in the programming mode.

10. The method of claim 5, including iteratively performing the calculation of the calibration value and the writing of the calibration value to the non-volatile memory.

11. A system to calibrate an oscillator within a radio-frequency identification (RFID) circuit for use in an RFID tag, the oscillator having an oscillation frequency and the system including:

first means, associated with the RFID circuit, for receiving a test signal; and

second means for storing a calibration value within a non-volatile memory associated with the RFID circuit,

wherein the second means is for recovering a reference frequency from the test signal, for calculating the calibration value to correspond to a difference between the recovered reference frequency and the oscillator frequency, and for writing the calibration value to the non-volatile memory.

12. A machine-readable medium storing a description of a circuit, said circuit comprising:

an input, associated with an RFID circuit, to receive a test signal; and

a calibration module to store a calibration value within a non-volatile memory associated with the RFID circuit,

wherein the calibration module is to recover a reference frequency from the test signal, to calculate the calibration value to correspond to a difference between the recovered

reference frequency and an oscillator frequency of an oscillator of the RFID circuit, and to write the calibration value to the non-volatile memory.

13. The machine-readable medium of claim 12, wherein the description comprises a behavioral level description of the circuit.

14. The machine-readable medium of claim 13, wherein the behavioral level description is compatible with a VHDL format.

15. The machine-readable medium of claim 13, wherein the behavioral level description is compatible with a Verilog format.

16. The machine-readable medium of claim 12, wherein the description comprises a register transfer level netlist.

17. The machine-readable medium of claim 12, wherein the description comprises a transistor level netlist.